User's Guide

SMB20 *Ardèche* – High-Speed Compensator

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Contents

1 Important Notice

The information given in this guide applies to the SMB20-R22A module. Information in this document is subject to change without notice.

2 Overview

The SMB20 module is an electronic board for use in Optical Phase-Locked Loop (OPLL) applications where the frequency detuning $\delta\nu$ between two laser sources requires tight and quick control.

This board is recommended to process the offset frequency error signal coming from the Phase/Frequency Discriminator module (SMB10). Designed for the high-speed path of the control loop, its output signal is intended to drive the fast frequency actuator device (the slave laser diode in OPLL). In order to avoid saturation of the high-speed loop, a low frequency path using a piezoelectric actuator may be required (see SMB30 module).

The SMB20 module offers a high performance compensator for the designers allowing a complete control of the loop filter operation. The polarity of the error signal is set either on board or using remote control. The loop gain is adjusted over more than 40 dB using the front panel trimmer or a DC-voltage. The length of the electrical path of the high-speed PID has been minimized while two additional integrator stages can boost the loop gain at low frequency. For lock-acquisition purposes, the integrator output of the fast PID can be precisely controlled by the user using a dedicated tracking input. A ramp input is also provided to sweep the laser frequency during the open-loop operation while the feedforward input offers a useful control of the fast actuator for frequency jumps or closed-loop measurements.

Like all SM-Series modules, the SMB20 is shipped with the schematic diagrams of its electronic circuitry, providing all required information for advanced users.

2.1 Fast PID

In fast PID mode, the **Servo Output** signal is given by

$$\text{Servo} = k\left(z + \frac{1}{T_\text{i}}\int z\text{d}t + T_\text{d}\frac{\text{d}z}{\text{d}t}\right) + \text{Ramp} + \text{Feeforward} \tag{1}$$

where z is the error signal and k, T_i, T_d are respectively the gain, the integrator and the differentiator time constants of the PID compensator. In frequency domain, this equation is equivalent to

$$\text{Servo} = kz\left(1 + \frac{2\pi f_\text{i}}{s} + \frac{s}{2\pi f_\text{d}}\right) + \text{Ramp} + \text{Feedforward} \tag{2}$$

where s is the Laplace variable. The unity gain frequencies $f_\text{i} = 1/2\pi T_\text{i}$ and $f_\text{d} = 1/2\pi T_\text{d}$ are selected using miniature on-board switches. The gain k is set using either a front panel potentiometer or a DC-voltage control input.

The PID compensator implemented in SMB20 differs in several points from the ideal transfer of above equations. First, the bandwidth of the differentiator is limited using two additional poles

$$\frac{s}{2\pi f_\text{d}} \rightarrow \frac{s}{2\pi f_\text{d}}\frac{1}{\left(1 + s/2\pi f_\text{d}^{'}\right)\left(1 + s/2\pi f_\text{d}^{''}\right)} \tag{3}$$

The cut-off frequencies $f_\text{d}^{'}$ and $f_\text{d}^{''}$ provide the high-frequency roll-off required to reduce the amplification of the noise one decade above f_d. The high-frequency gain of the differentiator is given by $f_\text{d}^{'}/f_\text{d}$. This gain is selected using a two-position switch located on board. By default, $f_\text{d}^{''}$ is not used.

The integrator path is also modified to provide passive filtering of high-frequency components present in the error signal. This is essential to avoid the DC-rectification that occurs when fast transients are applied to a slew rate limited active integrator. The integrator modification is given by

$$\frac{2\pi f_{\mathrm{i}}}{s} \rightarrow \frac{2\pi f_{\mathrm{i}}}{s} \frac{1}{1 + s/2\pi f_{\mathrm{i}}^{'}} \tag{4}$$

where the cut-off frequency $f_{\mathrm{i}}^{'} = 10\,\mathrm{MHz}$ by default.

2.2 Integrator Preset

The PID integrator output can be precisely controlled by the user using an internal closed-loop. Thus, during tracking mode operation, a dedicated input is copied onto the integrator output. This functionality can be useful during lock acquisition phases or once locking is lost to restore the previous operating conditions.

2.3 Additional Phase-Lead Filter

The phase lead provided by the differentiator path can be too small to ensure the stability of some closed-loops. If more phase lead is required, the servo output amplifier can be used to implement such circuit. By default, these phase lead components are not populated.

2.4 Additional Phase-Lag Filter

For some open-loop systems, the required proportional gain of the PID can be too small to preserve the input signal-to-noise ratio (SNR). For such high-gain systems, an additional phase-lag filter can be implemented using the feedback network of the PID summing amplifier. With this circuit correctly tuned, the proportional gain can be increased and the input SNR restored.

2.5 Extra Integrator Stages

In order to increase the loop gain at low frequency, two high-gain stages can be independently inserted before the fast PID. Once enabled, these extra integrators can lead to a PI^3D action. The operation bandwidth of these integrators should be limited to two octaves below the fast integrator frequency to preserve the initial stability. To avoid the introduction of additional delays, a parallel topology is used to connect the low frequency integrators. When the two extra gain stages are enabled, the change in the error signal can be approximated by

$$z \rightarrow z\left(1 + \frac{2\pi f_{\mathrm{i1}}}{s} + \frac{2\pi f_{\mathrm{i2}}}{s} + \frac{4\pi^2 f_{\mathrm{i1}} f_{\mathrm{i2}}}{s^2}\right) \tag{5}$$

3 Operation

3.1 Front Panel

There are a total of one SMA, three BNCs and one trimmer on the front panel, they are described in this section.

3.1.1 Servo Output SMA

Connect the fast frequency actuator with a 50-ohm coaxial cable. The output can be either a current or a voltage according to the output resistor ($R401$) populated. The **SERVO OUTPUT SMA** signal is a combination of the PID output, the ramp input and the feed-forward input

$$\text{Servo}\,(s) = z\,(s)\,\text{PID}\,(s) + \text{Ramp}\,(s) + \text{Feedforward}\,(s) \tag{6}$$

3.1.2 PID Monitor BNC

This BNC carries a copy of the PID signal. Connect a light load such an oscilloscope. Left open if not used.

3.1.3 Ramp Input BNC

Connect a signal generator to sweep the laser frequency during open-loop operation. This input is remotely controlled by the digital line /**RAMP** over the digital I/O interface. When ramp is on, the input signal is connected to the servo output amplifier through a differential stage. Can be left open if not used. For proper operation, any connections to the ramp pins of the analog interface should be removed.

3.1.4 Feed-Forward Input BNC

Connect a signal source for test or diagnostic purposes. This input is remotely controlled by the digital line /**FFWD** over the digital I/O interface. When feed-forward is on, the input signal is connected to the servo output amplifier through a differential stage. Can be left open if not used. For proper operation, any connections to the feed-forward pins of the analog interface should be removed.

3.1.5 Loop-Gain Adjust Trimmer

Use this trimmer to adjust the proportional gain of the PID. If the on-board switch SW203-1 is on, the trimmer is useless and the gain is controlled by the analog I/O interface.

3.2 AIO and DIO Interfaces

Like all SMB-Series modules, the SMB20 has two 50-pin stack-through headers acting as Analog I/O and Digital I/O interfaces. In this section each pin allocated to the SMB20 operation is described.

3.2.1 AIO Phase Error Input

Connect the error signal coming from the discriminator using the **(ERR-POS**, **ERR-NEG)** differential pair.

3.2.2 AIO Loop-Gain Input

Use the **(GAIN-POS**, **GAIN-NEG)** differential input to control the proportional gain of the PID. The on-board switch SW203-1 must be on to allow remote control. Can be left open if not used.

3.2.3 AIO Servo Output

This pin is directly connected to the **SERVO OUTPUT BNC**.

3.2.4 AIO Tracking Input

Use the **(TRACKING-POS, TRACKING-NEG)** differential pair to preset the integrator output voltage of the fast-PID. This input is remotely controlled by the digital line /**TRK** over the **DIO interface**. When tracking is on, an internal closed-loop copies the input tracking voltage onto the integrator output. Settling time is function of the integrator time constant. Can be left open if not used.

3.2.5 AIO Signal Ground

A clean signal ground **GND** is provided as a reference for measurements purposes. *Do not connect this pin to a ground signal*, use a differential sense circuit. Left open if not used.

3.2.6 AIO Ramp Input

Use the **(RAMP-POS, RAMP-NEG)** differential pair to sweep the laser frequency during open-loop operation. This input is remotely controlled by the digital line /**RAMP** over the digital I/O interface. When ramp is on, the input signal is connected to the servo output amplifier through a differential stage. Can be left open if not used. For proper operation, any connection to the **RAMP INPUT BNC** should be removed.

3.2.7 AIO Feed-forward Input

The **(FFWD-POS, FFWD-NEG)** differential pair gives the user a direct control of the laser frequency. This input is remotely controlled by the digital line /**FFWD** over the digital I/O interface. When feed-forward is on, the input signal is connected to the servo output amplifier through a differential stage. Can be left open if not used. For proper operation, any connection to the **FEED-FORWARD INPUT BNC** should be removed.

3.2.8 AIO PID Output

The pin carries a buffered copy of the **PID MONITOR BNC**. Can be left open if not used.

3.2.9 AIO Gain Output

This signal is a copy of the voltage applied to the voltage-controlled gain amplifier. Use the **GAIN OUTPUT** voltage to know the actual proportional gain. Can be left open if not used.

3.2.10 DIO Aux. Error Input

Connect the error signal coming from a different source using the **(AUX-ERR-POS, AUX-ERR-NEG)** differential pair.

3.2.11 DIO Gain-Boost-1 Input (/GB1)

This active-low input controls the operation of the first extra gain stage. For a logical 0, the gain stage behaves like a true integrator with an infinite DC-gain. For a logical 1, the circuit acts as a unity gain low-pass filter. When /**GB1** is left open, an internal pull-up resistor forces automatically the stage to operate in low-gain mode.

3.2.12 DIO Gain-Boost-2 Input (/GB2)

This active-low input controls the operation of the second extra gain stage. For a logical 0, the gain stage behaves like a true integrator with an infinite DC-gain. For a logical 1, the circuit acts as a unity gain low-pass filter. When /**GB2** is left open, an internal pull-up resistor forces automatically the stage to operate in low-gain mode.

3.2.13 DIO Gain-Boost Input (/GB)

For a logical 0, the input enables the extra gain stages whatever their operating mode. This allows PI^2D and PI^3D action. For a logical 1, the extra gain circuits are disconnected and the compensator acts as a fast-PID. An internal pull-up resistor disconnects automatically the extra gain stages when /**GB** is left open.

3.2.14 DIO Feed-Forward Input (/FFWD)

This active-low input controls the operation of the feed-forward signal. For a logical 0, the feed-forward signal is connected to the servo output and disconnected for a logical 1. An internal pull-up resistor disconnects automatically the feed-forward signal when the /**FFWD** is left open.

3.2.15 DIO Ramp Input (/RAMP)

This active-low input controls the operation of the ramp signal. For a logical 0, the ramp is connected to the servo output and disconnected for a logical 1. An internal pull-up resistor disconnects automatically the ramp signal when the /**RAMP** is left open.

3.2.16 DIO Tracking Mode Input (/TRK)

For a logical 0, the tracking mode is allowed. In this mode, an internal closed-loop copies the differential (**TRACK-POS**, **TRACK-NEG**) input voltage onto the fast-PID integrator. For a logical 1, the internal loop is removed and the integrator output operates normally. An internal pull-up resistor forces automatically the integrator in normal operation when the /**TRK** is left open. Use the tracking mode to restore locking conditions during lock-acquisition or frequency jumps.

3.2.17 DIO Integrator Input (/INT)

This active-low input controls the operation of fast PID integrator. For a logical 0, the integrator circuit acts as a true integrator with an infinite DC-gain. For a logical 1, the DC-gain is lowered and the integrator path behaves like a unity-gain low-pass filter. When /**INT** left open, an internal pull-up resistor forces automatically the integrator to operate in low-gain mode.

3.2.18 DIO Servo Input (/SERVO)

For a logical 0, the PID signal is connected to the servo output and disconnected for a logical 1. When the /**SERVO** is left open, an internal pull-up resistor disconnects automatically the PID signal from the servo output.

3.2.19 DIO Negative Polarity Input (/ERR)

When the input is set low, the error signal is applied to the PID circuit allowing closed-loop operation. The PID input is grounded if /**ERR** is set high. When /**ERR** is left open, an internal pull-up resistor

automatically disconnects the PID from the error signal. This input can be useful for lock acquisition purposes.

3.2.20 DIO Error (/NEG)

For a logical 0 (resp. 1), the polarity of the compensator transfer is negative (resp. positive). When /**NEG** is left open, the loop polarity is positive. To allow remote control of the polarity the on-board switch SW203-2 must be off.

3.2.21 Power Supply

The module needs analog ±15 V and digital +5 V power supplies. It is recommended to use the SMZ00 module to connect these sources.

3.2.22 Pin Assignments

The pin allocations of the **Analog I/O** and **Digital I/O** stack-through headers are given in Tables 1 and 2.

Signal label	Pin assignment	Direction
ERR-POS	AIO.38	input
ERR-NEG	AIO.40	input
LOOP-GAIN-POS	AIO.34	input
LOOP-GAIN-NEG	AIO.36	input
SERVO	AIO.28	output
TRACKING-POS	AIO.31	input
TRACKING-NEG	AIO.33	input
FEEDFORWARD-POS	AIO.35	input
FEEDFORWARD-NEG	AIO.37	input
RAMP-POS	AIO.30	input
RAMP-NEG	AIO.32	input
PID	AIO.27	output
GAIN	AIO.29	output
GND	AIO.39	output
−15 V	AIO.45	input
+15 V	AIO.47	input
AGND	AIO.49	input

Table 1: Analog I/O connector pin assignments.

3.3 On-Board Settings

3.3.1 Loop-gain Overdrive Selector (SW203-1)

Use this switch to allow remote control of the proportional gain. When the switch SW203-1 is on, the front panel trimmer is useless and the gain is controlled over the analog I/O interface. Set SW203-1 off if front panel adjustment is required.

Signal label	Pin assignment	Direction
AUX-ERR-POS	DIO.14	input
AUX-ERR-NEG	DIO.13	input
/NEG	DIO.32	input
/ERROR	DIO.30	input
/SERVO	DIO.38	input
/INT	DIO.31	input
/TRACK	DIO.34	input
/RAMP	DIO.29	input
/FF	DIO.36	input
/GB	DIO.37	input
/GB2	DIO.35	input
/GB1	DIO.33	input
+5 V	DIO.47 & DIO.48	input
DGND	DIO.49 & DIO.50	input

Table 2: Digital I/O connector pin assignments.

3.3.2 Gain-Boost#1 Unity-Gain Frequency (SW201)

Use the on-board switches SW201-2 as indicated in Table 3 to select the time constant of the first extra integrator stage.

SW201-2	SW201-1	Unity-Gain Frequency
off	off	150 kHz
off	on	50 kHz
on	off	15 kHz

Table 3: Selection of the Gain-Boost#1 unity-gain frequency.

3.3.3 Gain-Boost#2 Unity-Gain Frequency (SW202)

Use the on-board switches SW202-1 and SW202-2 as indicated in Table 4 to select the time constant of the second extra integrator stage.

SW202-2	S2W02-1	Unity-Gain Frequency
off	off	150 kHz
off	on	50 kHz
on	off	15 kHz

Table 4: Selection of the Gain-Boost#2 unity-gain frequency.

3.3.4 Integrator Unity-Gain Frequency (SW402-1, SW402-2, SW402-3)

Use the on-board switches SW402-1, SW402-2 and SW402-3 as indicated in Table 5 to select the time constant of the fast-PID integrator. The user defined value is set using C413 capacitor.

SW402-1	SW402-2	SW402-3	Unity-Gain Frequency
off	off	off	900 kHz
on	off	off	300 kHz
off	on	off	100 kHz
off	off	on	user defined

Table 5: Selection of the fast-PID Integrator unity-gain frequency.

3.3.5 Differentiator Unity-Gain Frequency (SW401-1, SW401-2, SW401-3)

Use the on-board switches SW401-1, SW401-2 and SW401-3 as indicated in Table 6 to select the time constant of the fast-PID differentiator. The user defined value is set using C406 capacitor.

SW401-1	SW401-2	SW401-3	Unity-Gain Frequency
off	off	off	3 MHz
on	off	off	1 MHz
off	on	off	300 kHz
off	off	on	user defined

Table 6: Selection of the fast-PID Differentiator unity-gain frequency.

3.3.6 Differentiator High-Frequency Gain (SW401-4)

Use the on-board switch SW401-4 to select the high-frequency gain of the derivative path. When SW401-4 is off (resp. on), the HF gain is set to +12 dB (resp. +20 dB).

3.3.7 Negative Polarity Selector (SW203-2)

Use the SW203-2 switch to set the polarity on the compensator transfer. When SW203-2 is on (resp. off), the polarity is negative (resp. positive). Setting SW203-2 off allows control of the polarity over the digital I/O interface.

3.3.8 Error Source Selector (R206-R207/R425-R426)

Use the resistors sets R206-R207 and R425-R426 to select the source of the error processed by the PID compensator. When R206-R207 are mounted (default), the error signal of the PID comes from the (AIO38, AIO40) differential pair. On the other hand, mount R425-R426 to operate the PID from the (DIO14, DIO13) differential pair.

4 Circuitry

4.1 Circuit Description

The error input signal is first applied to the differential amplifier U201. This error signal is selected between 2 sources using a pair of resistors (R206-R207/R425/R426). The error signal is then fed to the voltage controlled gain amplifier (VGA) U206 through two analog switches (U204A and U204B). The proportional gain of the fast-PID is adjusted by setting the VGA control voltage between 0 and 2 V. This control voltage is either supplied by the trimmer RV201 or the differential amplifier U203C whose inputs are connected to the

analog interface. The control voltage is buffered (U203A) and fed to the analog interface for measurement and diagnostic purposes.

The gain-boost stages are implemented using two integrators. A parallel topology is used to avoid additional delays that reduce the phase margin of the closed-loop. The first integrator (U203E) amplifies the error signal and drives the non-inverting input of the second integrator (U203D). This circuit has also its inverting input connected to the error signal. Both integrators are connected to the error signal through a passive low-pass filters (RA203/C212 and RA202/C211) to reject high-frequency components. The DC-gain boosters are controlled using analog switches (U202A and U202C). The unity-gain frequencies are selected using on-board switches (SW201 and SW202). The analog switch U202C (resp. U202B) enables the output of the second (resp. first) integrator. The output of the low-frequency gain circuit is applied to the analog switches of the VCA to implement the controlled phase inversion of the error signal.

The output of the VCA is connected to the fast-PID input through the analog switch U204D. In order to minimize delays, the PID action is split in 3 paths. The proportional action is implemented using the inverter U401A while the differentiator path is organized around U401C. The integrator is more complex and uses two operational amplifiers (U404E and U404D). Each P,I and D output is fed to the summing amplifier U402C to provide the PID signal. Once buffered, this signal is both connected to the analog interface header and to the front panel BNC.

An internal closed-loop including U405D and U404D copies the tracking input voltage onto the integrator output. The tracking operation is controlled by the analog switch U406A while U406D controls the integrator DC-gain. A low-pass filter (RA401 and C414) provides the attenuation of high-frequency components present in the error signal.

The high-frequency gain of the differentiator is set using R405 and R404 while C407 can provide an additional roll-off. The unity-gain frequencies are selected using the miniature switches (SW401-1 to SW401-3).

A phase-lag filter can be implemented using the feedback network (R406/C410) of the summing amplifier U402C. Additional phase-lead circuits are provided thanks to the R412/C411 or R403/C402 networks of the output amplifier U402A .

The PID signal is fed through the analog switch U403C to one of the three inputs of the inverting amplifier U402A. The remaining inputs are connected to the ramp and feed-forward signals that are enabled using the analog switches U403A and U403B. The feed-forward signal is fed using either the front panel BNC or the analog interface connector. The RA307 resistors provide current limitation if both BNC and interface voltages are unintentionally present. The isolation amplifier U405E avoids ground-loops.

The compensator operation is digitally controlled using the digital interface connector J201. Each digital input is buffered and pull-up resistors allow open-collector or open-drain control.

4.2 Printed Circuit Board Legend

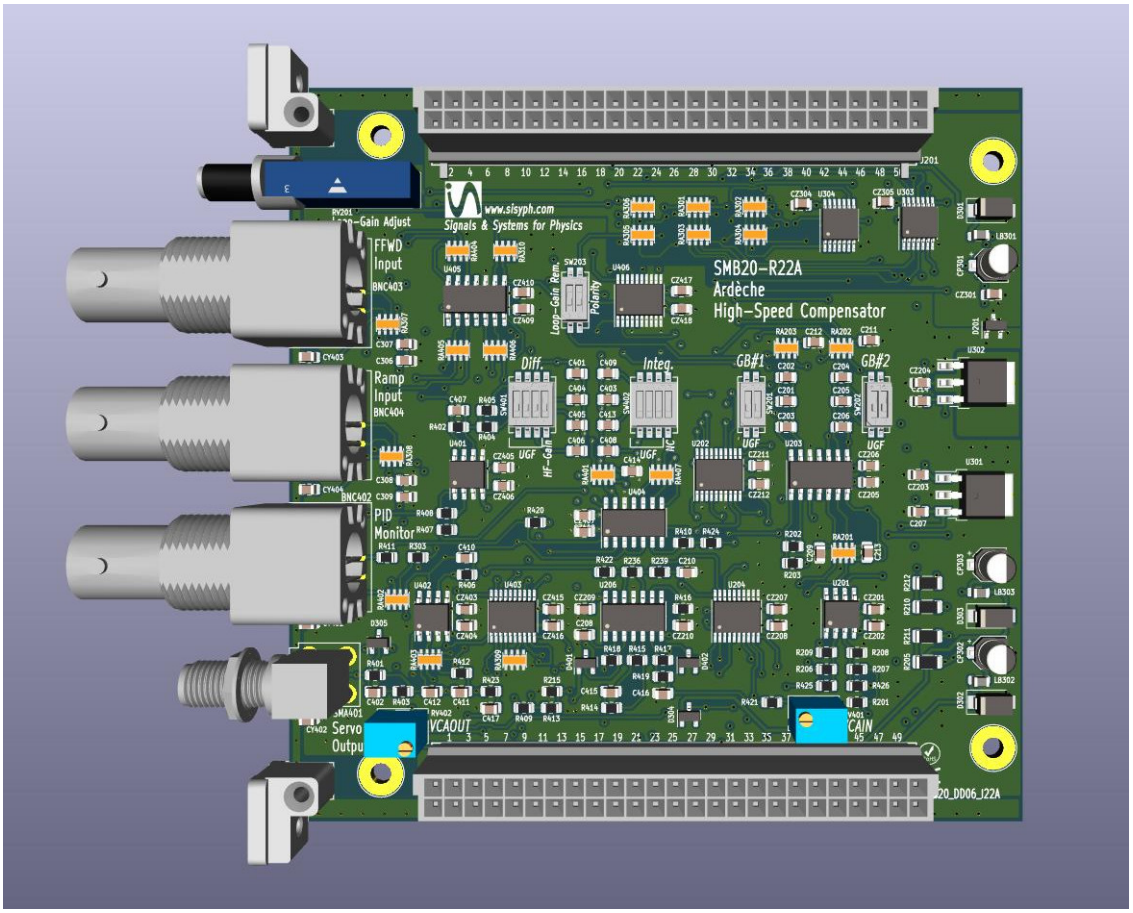

Figure 1: SMB20-R22A printed circuit board legend

Document Revision History

Release	Comments
SMB20-SN02-P22A	updated sections updated board legend