SK633 *Sancy* - Low-Noise Phaselock Controller

INPUTS

Reference

FP — SMA REFI

The Reference signal is fed from an external RF source and provides the phase reference to which the feedback signal is locked.

Feedback

FP — SMA FBKI

The Feedback signal is provided by an RF VCO or a laser beat note. Its phase is locked to the reference.

Low-Noise Phase-Frequency Detector

Matching Attenuator → Low-Pass Filter → Buffer → REF → Counter (FREF)

Matching Attenuator → Low-Pass Filter → Buffer → FBK → Counter (FFBK)

Both Reference and Feedback input paths use identical signal conditioning. A matching attenuator sets the input level and impedance, a low-pass filter removes unwanted high-frequency content, and a buffer provides the signal level and drive required by the phase detector.

Counters monitor the frequencies of the Reference and Feedback input signals with limited frequency resolution.

Phase/Frequency Detector

The phase/frequency detector compares the Feedback signal with the Reference signal and generates an output proportional to their phase difference.

PFD, XER ← XERE

XERI EXP — External Error Input
Auxiliary test port

The filter removes high-frequency ripple generated by the phase comparison.

Spurious Filter

ERR

Polarity Inverter

The polarity inverter sets the correct loop sign to ensure stable operation.

INVE

Low-Noise Analog Loop Filter

Offset

The Offset DAC allows the plant to be tuned or biased close to the locking point. It can also be used to remove the mean value from the loop-filter output.

OFSV → DAC → OFS ← OFSE

Main Loop-Filter

The loop-filter is implemented as a Proportional-Integrator compensator
The integrator should be engaged to preserve the PFD noise floor.
Fi ranges from 100Hz to 300kHz in 1–3 steps while Kp is fixed here (Kp=1).

INTF, INTE

Optional Loop-Filter

Additional pole-zero pairs can be added to the Main Loop-Filter for specific loop shaping.
The circuit diagram of this section is available on request for advanced users.

MLF, 0V, OLF → MUX ← CMDS

0V

Limiter – Lock Detection

The command limiter protects the frequency actuator by constraining the control voltage within programmable safe limits.
Its internal window comparator is also used as a lock indicator, with Voltage Lock Detection asserted while the command voltage remains within the allowed range.

CMDE, LIMP, LIMN → CMD

VLD, CMD

EFB → MUX → MONS

MLF, EFB, ELF, EAC

Error Monitoring

Band-limited copies of the error signal are provided for monitoring purposes.

ERR

Signal Bus

Signal Monitoring

ELF → MUX → ADC → STMN, STME

Post-Processing & Remote Monitoring

OUTPUTS

CMDO — SMA CMDO — EXP, UTB, FP

Command

The frequency actuator (e.g. VCO) is connected to the Command output to complete the phase-locked loop.

MONO — SMA MONO — EXP, UTB, FP

Monitoring

The Monitoring output provides copies of selected internal signals.

FRONT-PANEL DISPLAY

Phase-Freq. Detector

CM	FP	Command output enabled
LD	FP	Lock-detector asserted
xx	FP	Reserved
LM	FP	Command limiter engaged
MS	FP	MSS status bit set
FT	FP	Fault condition detected
RA	FP	Activity detected
RE	FP	Error detected

Static Led Driver

SPI

Remote Control

MISC.

DIOs

UTB, EXP: DIO{0,1}

Reserved for future use.

Firmware Cfg Switches

PCB: FCFG{0-3}

Reserved for future use.

Micro-Controller

GPIO, GPIO, SPI, GPIO, I2C, UART, GPIO, GPIO, GPIO

MCU Bus: ADC, DAC, Led Driver... / Mux, Switch...

/STATUS, 0V

Reverse/Over-Voltage & In-Rush Current Protections

REMOTE CONTROL

BKP /STATUS
BKP I2C{SDA,SCL}
BKP UART{RX,TX,/CTS,/RTS}
BKP /SLOT
BKP ID{0-3}

The module is controlled through these lines.

POWER SUPPLIES

BKP {P15V,N15V,AGND}
BKP {P24V,P5V,N5V,DGND}
BKP PWRGD

The module is powered *via* these lines.

PRELIMINARY INFORMATION

- Only main functionalities are represented. Refer to the *User's Guide* for detailed information.
- Refer to the *User's Programming Guide* for a complete description of the remote control commands.

Symbols

Testpoint	
Coaxial connector	
I/O	
Indicator	
CMD Command	
Jumper	

Locations

PCB	Printed circuit board
BKP	Backplane connector
UTB	User's terminal blocks
EXP	Expansion connector
FP	Front panel

Domains

Optical
Microwave
RF
Analog (LF)
Digital (LF)

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Signals & Systems for Physics
www.sisyph.com
206 rue Alfred Kastler
17190 Saint-Georges-d'Oléron
FRANCE

Title/Name: SK633 *Sancy* - Low-Noise Phaselock Controller	Release: SK633-R26A
Description: Functional block diagram.	
Drawing No.: SK633-SG01-P26A	

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